DETAILED ACTION

1. This action is responsive to the amendment filed on October 13, 2009.

2. Claims 17 and 31-37 have been examined.

Response to Arguments

3. Applicants' arguments have been fully considered.

a) Applicants asserted,

> "Ballagh's Figure 2 illustrates a circuit design 200 including an FPGA 202 that communicates with an external processor. The functional requirements of the circuit design 200 are described at column 5, lines 4-38. <u>That circuit design 200 does not perform a numerical simulation</u>." (Remarks, page 3, first full paragraph, emphasis added).

As an initial matter, examiner would like to direct Applicants' attention to well-known definitions:

floating-point

(flō'tĭng-point')

adj.

Of, relating to, or being a method of writing numeric quantities with a mantissa representing the value of the digits and a characteristic indicating the power of the number base, such as 3×10^{-5}.

fixed-point

(fĭkst'point')

adj.

Of, relating to, or being a method of writing numerical quantities with a predetermined number of digits and with the decimal located at a single unchanging position.

binary point

('bīn·ə·rē 'pȯint)

(*computer science*) The character, or the location of an implied symbol, that separates the integral part of a numerical expression from its fractional part in binary notation.

Examiner notes that the full pages of these definitions extracted from the website Answers.com have been attached with this Office action.

Ballagh teaches:

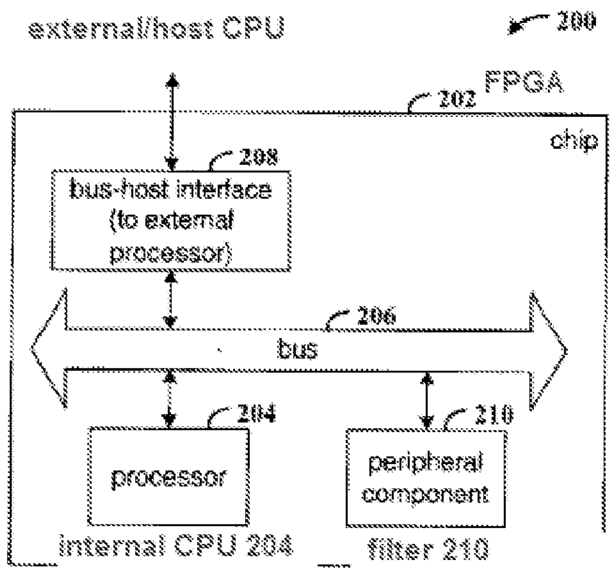
"using the CPU to perform a numerical simulation" (e.g., representing sample rates, data precision as arithmetic values using floating point and/or fixed point and simulating said floating point and/or fixed point, i.e., "numerical simulation" as claimed). For example:

> "The modeling phase consists of capturing the design in an executable form, simulating, then analyzing the results. The modeling phase is appropriate for algorithm exploration, in which system parameters such as sample rates, data precision, and choice of functional blocks are decided. This process is iterative, with the results of analysis leading to revisions that allow system specifications to be met. In the modeling phase, a high level of abstraction is desirable in order to facilitate algorithm exploration. For example, it is common to represent arithmetic values using floating point or fixed point rather than as buses of logic signals. Sampled data systems are also most conveniently modeled by defining sample rates rather than using explicit interconnections ("wires") representing clock and associated control signals (e.g., enable, reset)." (col.1: 32-46, emphasis added).

"including generating input signals and sending the input signals to the FPGA" (e.g., FIG. 2, external/host CPU transfers new coefficients to FPGA 202 via bus interface 208, wherein FPGA 202 including filter 210 which processes/supports

"coefficient precisions" and "coefficient binary point", i.e., FPGA 202 process/perform "numerical simulation" as claimed). For example:

> "A hardware realization of design 200 operates in two modes: filter reloading and filter frame data transfer. When the filter (i.e., the peripheral component) is not being reloaded, frames of filter output are transferred over the bus to (internal) processor 204. The frames are then sent from the processor on *bus* 206 to a host computer for analysis. On the host (external/host CPU), the user may construct a new filter and transfer new coefficients to the (internal) processor via bus interface 208 and bus 206. Upon receiving the coefficients, the (internal) processor transfers the coefficients to the peripheral component (filter 210).
>
> ...
>
> The library element that defines the filter also supports parameterization of the coefficient precision, coefficient binary point, number of taps, and filter oversampling rate. The example filter is configured with 32 taps, 12-bit coefficient precision, and reloadable coefficients." (col.5: 29-54, emphasis added).



annotated **FIG. 2**

b) Applicants further asserted,

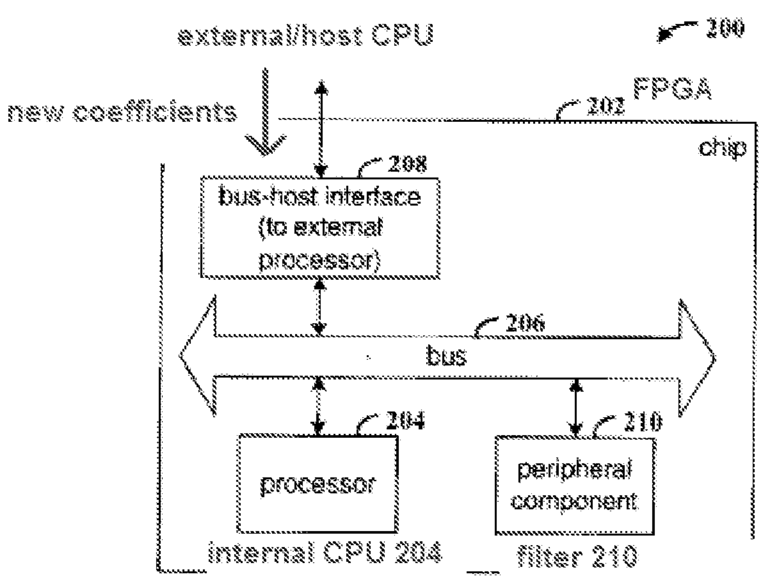
> "Ballagh does not teach or suggest offioading a portion of the simulation from a computer to an FPGA. It follows that Ballagh is also silent about data flow between a computer running a portion of a numerical simulation and a FPGA running another portion of the numerical simulation." (Remarks, page 3, last full paragraph).

As an initial matter, examiner notes that the plain language of claim merely recites "<u>using the CPU</u> to perform a numerical simulation including generating input signals and <u>sending the input signals to the FPGA</u>" (claim 31, lines 4-5, emphasis added).

As addressed in a) above and further recited below, Ballagh teaches sending new coefficients ("sending the input signals to the FPGA" as claimed) from external/host CPU to FPGA 202. For example:

"…In an example application, the host computer (host/external CPU) initiates filter reloading and transfers new filter coefficients to processor 204 (i.e., internal processor embedded in FPGA 202). Upon receiving new coefficients from the host (external/host CPU), the (internal) processor controls the filter reloading from within the FPGA.

A hardware realization of design 200 operates in two modes: filter reloading and filter frame data transfer ... On the host (i.e., external/host CPU), the user may construct a new filter and transfer new coefficients to the (internal) processor (i.e., embedded in FPGA 202) via bus interface 208 and bus 206…" (col.5: 24-36, emphasis added).



annotated **FIG. 2**

Accordingly, dependent claims 17 and 32-34 are also rejected based on virtue of their dependencies on the rejected base claim 31.

Claims 35-37 are also rejected as addressed in a) and b) above.

Claim Rejections – 35 USC §102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 31 is rejected under 35 U.S.C. 102(e) as being anticipated by Ballagh (art of record, US Patent No. 6,883,147).

Claim 31:

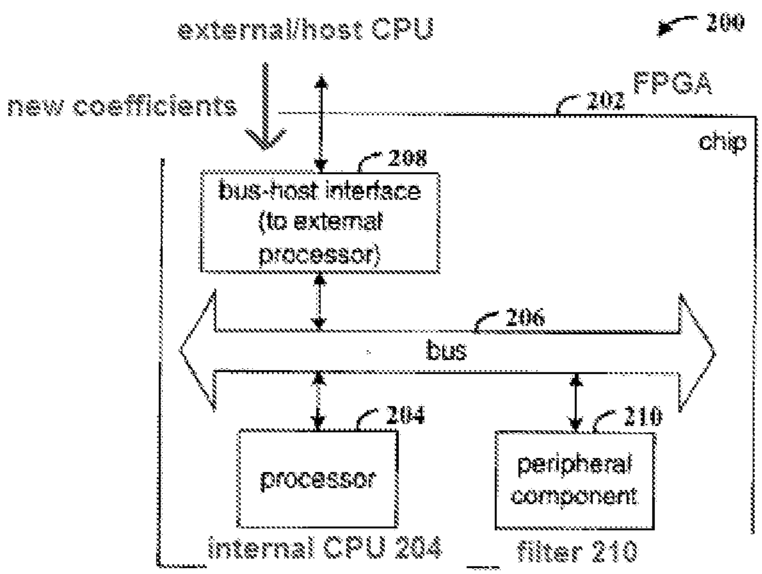
Ballagh discloses *a method of performing a numerical simulation with a Field Programmable Gate Array (FPGA) and a separate central processing unit (CPU), the method comprising:*

using the CPU (e.g., FIG. 2, an “external processor” (host CPU) coupled to bus-host interface 208, col.5: 22-28)

to perform a numerical simulation including generating input signals (e.g., col.4: 47-64, the host CPU and a system-level simulation environment 110) *and*

a FPGA (e.g., FIG. 2, chip 202, which is “an FPGA from Xilinx”, col.5: 6-9)

sending the input signals to the FPGA (e.g., col.5: 28, from the external processor (host computer/CPU), transferring new filter coefficients to processor 204 (embedded within chip/FPGA 202))*;*



annotated **FIG. 2**

using the FPGA to apply a model to the input signals (e.g., FIG. 2, col.5: 6-14, chip/FPGA 202 has peripheral component 210, which includes a reconfigurable digital filler to process the input signals, col.5: 19-22; FIG. 3A, col.5: 39-54, said reconfigurable digital filter has specific "control logic that manages coefficient reloading, adjusts data rates, and controls filter output frame buffering", i.e., applying a specific model to the input signals) *and send results of the model back to the CPU* (e.g., col.5: 29-34)

the FPGA also generating a first output that marks data as valid or invalid (e.g., FIG. 3A, FPGA 202 generating "coef_we" (first output) to mark "coef" valid or invalid and sending "coef_we" to its sub-component FIR filter 250, col.5: 55-65),

a second output that indicates the first sample of each frame (e.g., FIG. 3A, output port "yn" indicating data in output frames, col.5: 29-38 and 43-48)*, and*

a third output that indicates when the model can accept data (e.g., FIG. 3A, FPGA 202 generating "rfd" indicating status "busy" or not, col.5: 55-65)*; and*

wherein the CPU uses the results in the numerical simulation and the outputs to maintain data flow with the FPGA (e.g., col.6: 30-39, when the FIFO is full,

initiating a filter reload sequence and issuing read requests to obtain new coefficients from the external processor, col.5: 34-38).

Claim Rejections – 35 USC §103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballagh in view of APA (art of record, Admitted Prior Art).

Claim 32:

Ballagh does not explicitly disclose *the method of claim 31, wherein the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a FFT.*

However, in an analogous art, APA further discloses *the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a FFT* (e.g., page 2: 4-23).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to transform a digitized waveform in the time domain into a digital representation in the frequency domain using Simulink simulation software as suggested by APA (e.g., page 2: 5-9 and 20-23).

Claim 33:

Ballagh discloses *the method of claim 32, wherein the FPGA converts inputs from double point precision to fixed point prior to performing the transform* (e.g., col.3: 52-65; col.5: 29-38)*; and wherein the FPGA converts the results from fixed point back to double precision prior to sending the results back to the CPU* (e.g., col.4: 65 – col.5: 38; col.6: 47-65).

APA further discloses *the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a FFT* (e.g., page 2: 4-23).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to transform a digitized waveform in the time domain into a digital representation in the frequency domain using Simulink simulation software as suggested by APA (e.g., page 2: 5-9 and 20-23).

Claim 34:

APA further discloses *the method of claim 32, wherein the CPU performs a numerical simulation of a radar system* (e.g., page 2: 4-15).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to as set forth above.

Claim 35:

Ballagh discloses *an apparatus* which recite(s) the same limitations as those of claim 31, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the reference teaches all of the limitations of the above claim(s), it also teaches all of the limitations of claim 35.

APA further discloses *a numerical simulation of sine wave functions representing real and imaginary inputs; and performing an FFT on the inputs* (e.g., page 2: 4-23).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to transform a digitized waveform in the time domain into

a digital representation in the frequency domain using Simulink simulation software as suggested by APA (e.g., page 2: 5-9 and 20-23).

Claim 36:

Ballagh discloses *the apparatus of claim 35, wherein the FPGA converts the real and imaginary inputs from double point precision to fixed point prior to performing the transform* (e.g., col.5: 1-38; col.6: 47-65)*; and*

wherein the FPGA converts the results of the FFT from fixed point back to double precision prior to sending the results back to the CPU (e.g., col.3: 52-65; col.4: 65 – col.5: 38).

Claim 37:

APA further discloses *the apparatus of claim 35, wherein the CPU performs a numerical simulation of a radar system* (e.g., page 2: 4-15).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to as set forth above.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ballagh in view of APA and Ozawa (art of record, US Patent Publication No. 2002/0103839 A1).

Claim 17:

The rejection of claim 32 is incorporated. Ballagh discloses *coupling an output of a double delay block to a third input of the FFT block, the third input being adapted to mark data input as valid or invalid* (e.g., FIG. 3A, FPGA 202 generating "coef_we" (first output) to mark "coef" valid or invalid and sending "coef_we" to its sub-component FIR filter 250, col.5: 55-65).

APA further discloses *performing receiving the real and imaginary inputs at first and second inputs of an FFT block via a pair of gateway in blocks* (e.g., page 2: 4-23).

Neither Ballagh nor APA explicitly discloses other limitations. However, in an analogous art, Ozawa discloses:

coupling an output of a k=0 block to a fourth input of the FFT block (e.g., [0166] and [1203]),

the fourth input being adapted to control a forward or a reverse transform (e.g., [0351], performing cascade processing signals);

coupling outputs of FFT block to at least one D flip flop-based registers adapted to provide a signal latency; and coupling the outputs of the registers to at least one gateway out (e.g., [1268]-[1269]).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Ozawa's teaching into Ballagh and APA's teaching. One would have been motivated to do so to process data in an arithmetic device as suggested by Ozawa (e.g., [0007]-[0011]).

Conclusion

9. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication should be directed to examiner Thuy (Twee) Dao, whose telephone/fax numbers are (571) 272 8570 and (571) 273 8570, respectively. The examiner can normally be reached on every Tuesday, Thursday, and Friday from 6:00AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Twee Dao/
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Supervisory Patent Examiner, Art Unit 2192